

February 9, 2004

To: Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Req. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/755,495 01/12/04

Wei-Hua Cheng et al.

ADJUSTABLE 3D CAPACITOR

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

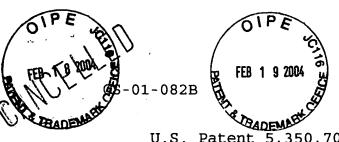
The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February | 7, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date



- U.S. Patent 5,350,705 to Brassington et al., "Ferroelectric Memory Cell Arrangement Having a Split Capacitor Plate Structure," discloses a flat capacitor arrangement with common top plate.
- U.S. Patent 6,088,258 to Aitken et al., "Structures for Reduced Topography Capacitors," discloses planarized interweave capacitor.
- U.S. Patent 5,604,145 to Hashizume et al., "Method of Manufacturing DRAM Capable of Randomly Inputting/Outputting Memory Information at Random," discloses a planar capacitor process.
- U.S. Patent 5,744,385 to Hojabri, "Compensation Technique for Parasitic Capacitance," reveals a compensation technique for a parasitic capacitor.

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

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